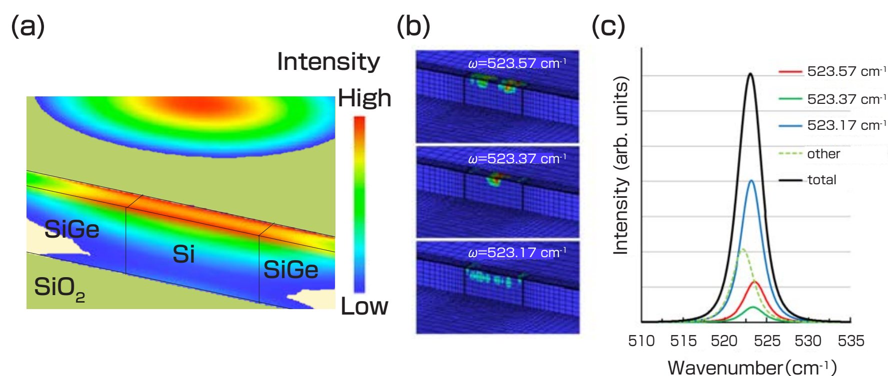
Three-dimensional stress analysis simulator for ultra-small silicon devices

Analysis at nanometer level using an optical microscope

We have developed a three-dimensional stress analysis simulator for ultra-small silicon (Si) devices. The developed simulation technology allows the analysis of the distribution of the mechanical stress (or mechanical strain) applied to ultra-small Si devices with a spatial resolution at the nanometer level by calculating the modulation of light intensity distribution caused by the device structure in the micro-Raman spectroscopy measurement using an optical microscope.



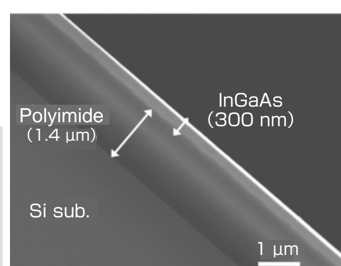
(a) Intensity distribution of excitation light calculated by the developed system
(b) Raman scattering light of each wavelength from the sidewall
(c) Spectrum of each scattering light obtained from the analysis and the combined Raman spectrum

Tetsuya TADA
Nanoelectronics Research Institute
t-tada@aist.go.jp
AIST TODAY Vol.13 No.3 p.9 (2013)

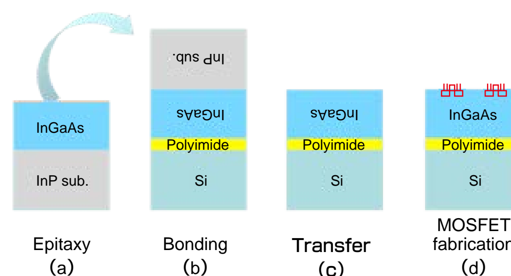
High performance transistors on polymer

A back-end integration technology for post-silicon materials

We have developed a technology for the transfer of a high performance compound semiconductor layer onto a silicon substrate using an inexpensive heat-resistant polymer as an adhesive. Transistors superior to silicon transistors were fabricated at maximum process temperatures as low as 400 ℃ on the polymer. Using the layer transfer and low-temperature device fabrication technologies, the realization of high-performance, multifunction devices integrating post-silicon materials with silicon large-scale integrated circuits is expected.



Cross-sectional SEM image of InGaAs layer on polyimide



Fabrication method of transistors on polyimide

Tatsurou MAEDA
Nanoelectronics Research Institute
t-maeda@aist.go.jp
AIST TODAY Vol.13 No.3 p.10 (2013)