Universal design with robots

Making robots more adaptable to human living environment

AIST has developed several elements of universal design for household robots in particular, with the cooperation of Takasuke Sonoyama of T-D-F/Robot & Interaction Design. This research was jointly conducted by the University of Tokyo, Toshiba Corp. and GNSS Technologies, Inc. in the project organized by the Next-generation Robots Coordination Program, Council for Science and Technology Policy - Coordination Program of Science and Technology Projects.

In conventional robotic development, a robot is built for a specialized purpose because its hardware is designed for a specific environment, and it is required to execute only a predetermined task. In practice, it is very difficult to develop a robot that can handle all items found in a human living environment. To overcome this difficulty, AIST devised some methods, as part of the environmental platform for the easy adaptation of robots to the human living environment in which humans and robots can coexist. The methods include designing handles that are easily operable by robots and also by human, designing visual marks in order to provide the layouts and operating instructions of the handles, and building templates for the easy development of operation programs for robots. Introduction of robots in households is expected to be accelerated by the popularization of these methods.

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Universal handle & CLUE (Coded Landmark for Ubiquitous Environments)

Novel SRAM circuit using double-gate-MOSFET devices

Promising solution for operational-stability enhancement in 22-nm generation

We have developed a fin-type-field-effect-transistor- (FinFET-) based SRAM to enhance noise margin during both read and write operations. In its cell, the flip-flop is composed of usual three-terminal- (3T-) FinFETs while the pass gates are composed of four-terminal- (4T-) FinFETs. The 4T-FinFETs allow dynamic threshold-voltage control in the pass gates. During the write operation, the threshold voltage of the pass gates is lowered to enhance the writing speed and stability. During the read operation, on the other hand, the threshold voltage is raised to enhance the static noise margin. This novel SRAM circuit is a promising solution to the chip-yield problem in 22-nm generation, which is caused by the shortage of the noise margin or the operational stability.

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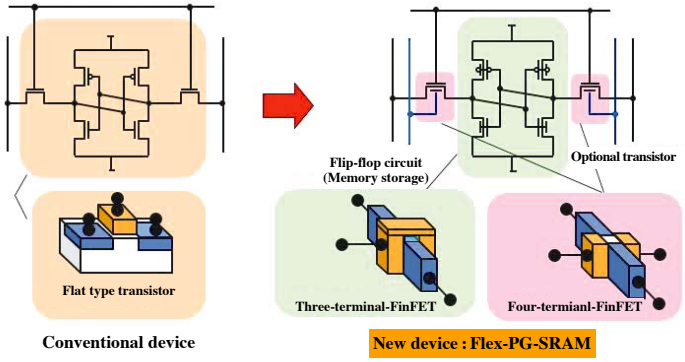

Comparison of circuit structure and device of conventional and new SRAM